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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2 Application Serial No. .... 08/530,661  
Filing Date ..... September 20, 1995  
3 Inventor ..... Brent Keeth  
Assignee ..... Micron Technology, Inc.  
4 Group Art Unit ..... 2503  
Examiner ..... N. Kelly  
5 Attorney's Docket No. .... MI22-356  
Title: Semiconductor Memory Circuit  
6

7 RESPONSE TO MARCH 19, 1997 OFFICE ACTION ~~REED~~

8 To: BOX NON-FEE AMENDMENT JUL 17 1997  
Assistant Commissioner For Patents  
9 Washington, D.C. 20231 GROUP 2503

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13 AMENDMENTS

14 In The Claims.

15 27. (Once amended) The semiconductor memory device of  
16 claim 6 wherein the peripheral circuitry, the pitch circuitry, and the  
17 memory arrays are fabricated to include a total of four or less  
18 [composite] conductive line layers.

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20 28. (Once amended) The semiconductor memory device of  
21 claim 6 wherein the peripheral circuitry, the pitch circuitry, and the  
22 memory arrays are fabricated to include at least five [composite]  
23 conductive line layers, the occupied area of all functional and operable